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Low-Power Heterogeneous Encoder Based 4-Bit Flash ADC Using TIQ

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Abstract: **Analog to digital conversion is an electronic process that converts a voltage that varies among a infinite number of values to a defined level or status. In this paper Heterogeneous encoder is proposed. Flash ADC structure is faster in digital conversion and use resistor ladder to compare between the input voltages and reference voltages. These designs consume more power and also have more delay. Therefore threshold inverter quantization (TIQ) based comparator has been introduced. TIQ technique uses the two cascading inverter as voltage comparator followed by a encoder, it provides the reduction in power and mostly use in battery operated devices. The heterogeneous encoder is proposed in this paper to get higher speed and to reduce power consumption. The Simulated results with 180nm CMOS technology in CADENCE VIRTUOSO platform shows that the proposed design achieves high speed and low power consumption compared to other analog to digital converters.**

Keywords: **Analog to Digital Converter, Flash ADC, Threshold inverter quantization, Encoder.**

I. INTRODUCTION

Analog-to-Digital converter(ADC) is a necessary section within the style of mixed signal, system on chip and signal process application[1].Power consumption, minimal space are the foremost needed standard due to exponential growth of battery operated and transportable devices like mobile phone, laptops, tablets and medical instruments. There are different types of ADCs is developed depending upon the types of applications. Based on various topologies different types of ADCs are: Flash ADC, Sigma delta ADC, Pipelined ADC, Successive approximation ADC [2]. Flash ADC (shows in fig 1) is known for quicker converter in among all the ADCs. N-bit flash ADCs consists of 2^N-1 resistor ladders, comparator and a encoder. The input signal is fed to the 2^N-1 comparator. N is the resolution of the ADC.A reference voltage is also provided to each comparator that is generated by resistor strings used in flash ADC. Comparators compare the input voltage with reference voltage generated by resistor ladder circuit, if input voltage become larger than the reference voltage then the output is HIGH otherwise the output is LOW. Flash ADC comparators gives the output in a continuous pattern of 1's and 0's, this pattern is known as Thermometer code. The thermometer code is then alter into binary code by(2^N-1) to N encoder. There are several encoder proposed by researchers to reduce the hardware complexity[3]. In this paper Threshold Inverter Quantization(TIQ) technique[4] is used to scale back chip space and also a new encoder circuit design is proposed to convert the thermometer code into binary code that minimize the power consumption compare to Wallace ,fat tree and existing MUX based encoder. This paper is unionized as follows: section II describes the TIQ flash ADC architecture, section III gives the detail about the different kinds of existing encoder and section IV provides the description of proposed heterogeneous encoder. Section V gives the simulation result of proposed heterogeneous encoder.

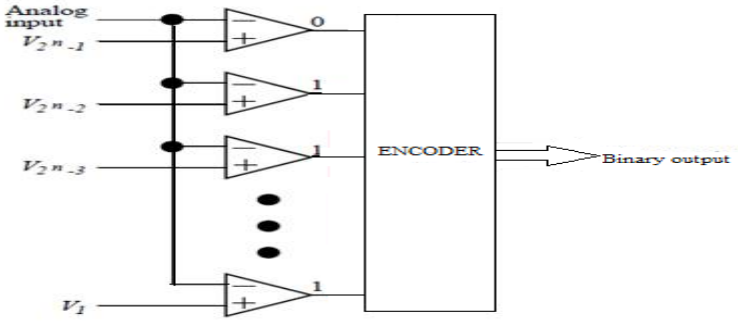

Fig. 1. Illustration of Flash ADC

II. TIQ FLASH ADC ARCHITECTURE

In N bit Flash ADC 2^N-1 comparator is employed to compare the reference voltage with the input voltage to induce the thermometer code. Here resistor ladder is employed to generate reference voltage. This design is complex and additionally consumes more power and area. Threshold Inverter Quantization(TIQ) technique is alternative approach to reduce the power consumption and chip area, it is basic CMOS inverter consists of one PMOS and one NMOS transistor with the switching threshold voltage[5].TIQ comparator made up of two cascade CMOS inverter where the first inverter is use to set the reference voltage of comparator by varying the width and length of the PMOS and NMOS transistor whereas the second inverter increases the voltage gain and manage linearity balance for the voltage rising and falling intervals of high frequencies input signals. Threshold of CMOS inverter (V_M) is a point where input voltage is equal to the output voltage (V_{IN} =V_{OUT}) in voltage transfer characteristics (VTC).At this time each transistor PMOS and NMOS invariably operate in saturation region. V_M can mathematically expressed as:

$$V_M = \frac{r(V_{DD} - |V_{Tp}|) + V_{Tn}}{1 + r}$$

Assume that the channel length of the PMOS and NMOS transistor (L_N = L_P) and gate oxide capacitance (C_{OX}) are same and V_{Tp} and V_{Tn} are the threshold voltages of PMOS and NMOS transistors respectively and

$K_n = (W/L)_n \cdot \mu_n C_{OX}$

$K_p = (W/L)_p \cdot \mu_p C_{OX}$

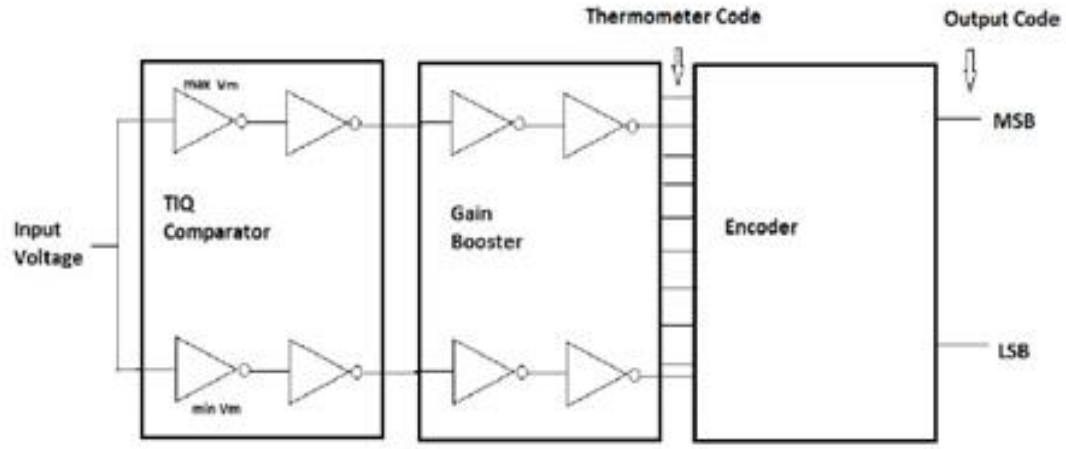

Fig 2: Block diagram of TIQ ADC

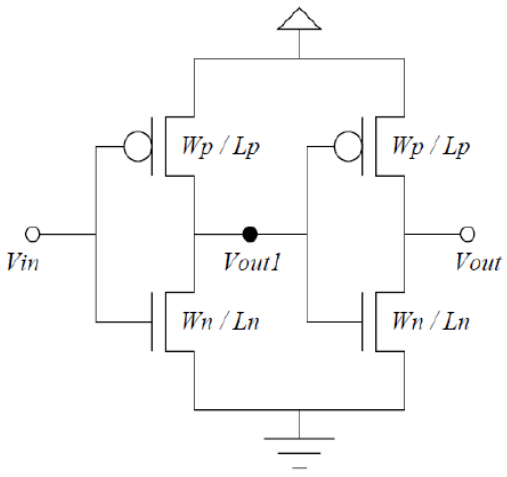

Fig 3: TIQ Comparator

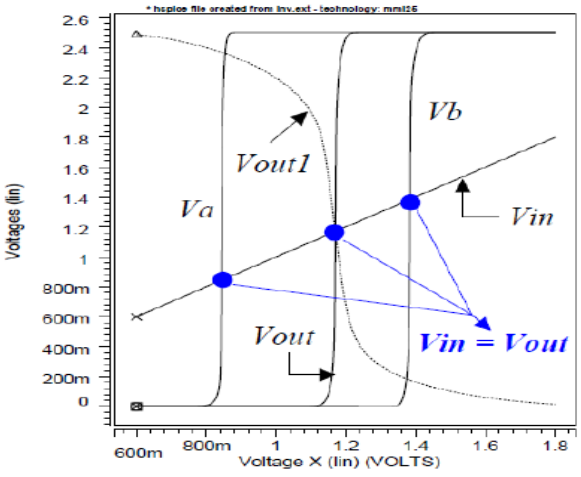

Fig 4: VTC of TIQ Comparator

V_M depend on the ratio of width of PMOS and NMOS (W_p / W_n), hence increasing of W_p makes the V_M larger and increasing W_n makes the V_M smaller as shown on the VTC. TIQ comparator generates the sharper threshold for comparator output and provides a digital output. If the analog input voltage is higher than the threshold voltage the digital output is logic "1" otherwise digital output is logic "0". The TIQ technique has several benefits like[6].

- The voltage comparator circuit is simple.
- Comparison rate is high.
- Eliminates the use of resistor ladder network.
- It does not require any clock signal for the voltage comparison.

III. EXISTING ENCODERS

A. ROM based encoder:

The output of comparator is thermometer code. ROM based encoder is the common approach to encode thermometer code into digital output[7]. The encoder functions in two stages, at first stage an array of NAND gate are used to convert thermometer code into 1 out of 2^N-1.The output of first sage is fed to the second stage where it selects the suitable row in the ROM structure. This approach is simple and straight forward to design, but delay and power consumption is more due to a static current used to preset the ROM encoder[8]. Bubble error is also an important issue of this design if the number of 1s is more than one out of 2^N-1 code then more than one row in the ROM will be enable which gives the erroneous binary code.

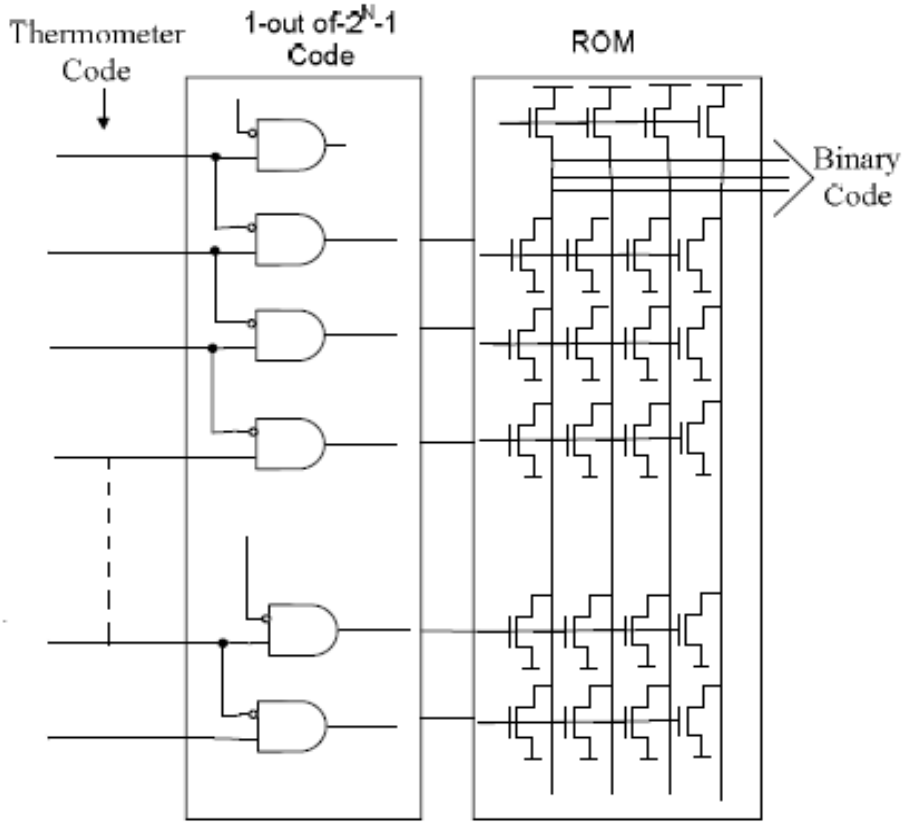

Fig.5: ROM based encoder

B. Wallace tree encoder:

Wallace tree encoder [9] is extremely uncomplicated approach which counts the number of 1's. The Wallace tree based decoder counts the number of number of 1s. This is useful for bubble Suppression. Large delay and power are the disadvantage of this approach [3][9].

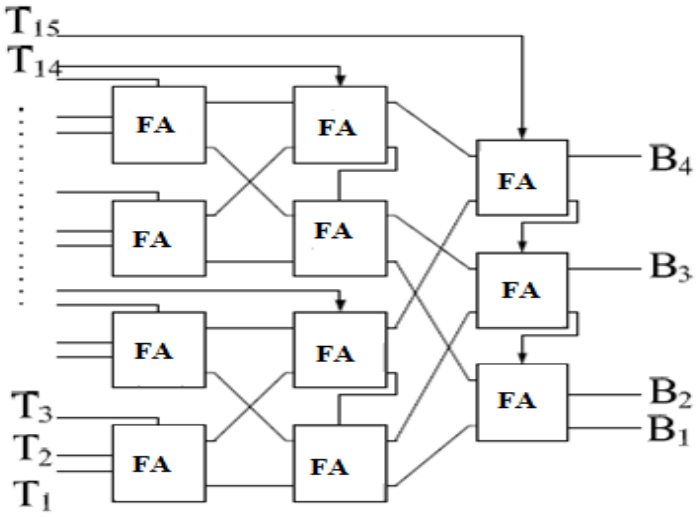

Fig.6: Wallace tree encoder

C. Fat tree encoder:

Wallace tree structure takes more space and delay compare to FAT tree encoder[10]. FAT tree structure has two stages.

The first stage converts the thermometer code to 1 out of 2^N-1 code and at the second stage multiple trees of OR gate is used to convert the 1 out of 2^N-1 to binary code. A more optimized implementation of the FAT tree based encoder is presented in[11]. This approach reduces the array of OR gate into NAND-NOR pairs. The NAND- NOR gates are implemented using a pseudo dynamic CMOS logic.

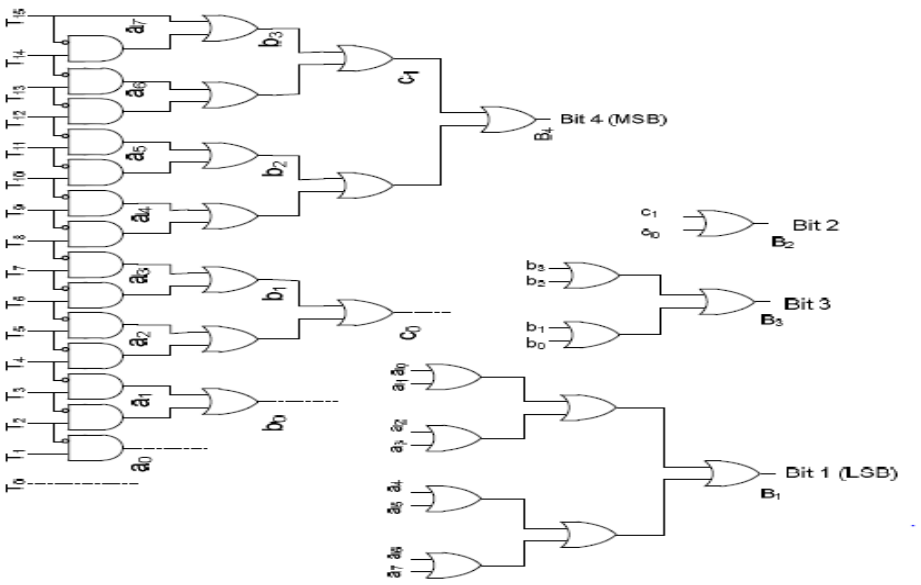

Fig.7: Fat tree encoder

D. MUX based encoder:

Fig 8 shows the implementation of MUX based encoder[12].Thermometer scale is divided into two partial thermometer scales, separated by the output at level 2^N-1. MUX based encoder operates at high speed and covers the small chip area compare to the Wallace and Fat tree encoders. The disadvantage of this approach is huge fan-out in the critical path, this result in increased power consumption and delay. A new modified implementation of MUX based encoder[13][14] is shown in fig 9. This encoder is implemented by grouping the results of smaller length MUX based encoder to develop a high bit resolution encoder to convert thermometer code in to binary output. It gives better result than previous encoders in terms of power consumption, speed and space. The Boolean expressions of output of the improved MUX based encoder are as follows:

$B_4 = T_8$

$B_3 = T_8.T_{12} + \bar{T}_8.T_4$

$B_2 = T_8(\bar{T}_{12}.T_{10} + T_{12}.T_{14}) + \bar{T}_8(\bar{T}_4.T_2 + T_4.T_6)$

$B_1 = \bar{T}_8[\bar{T}_4.(\bar{T}_2.T_1 + T_3.T_2) + T_4.(\bar{T}_6.T_5 + T_6.T_7)] + T_8[\bar{T}_{12}(\bar{T}_{10}.T_9 + T_{10}.T_{11}) + T_{12}.(\bar{T}_{14}.T_{13} + T_{14}.T_{15})]$

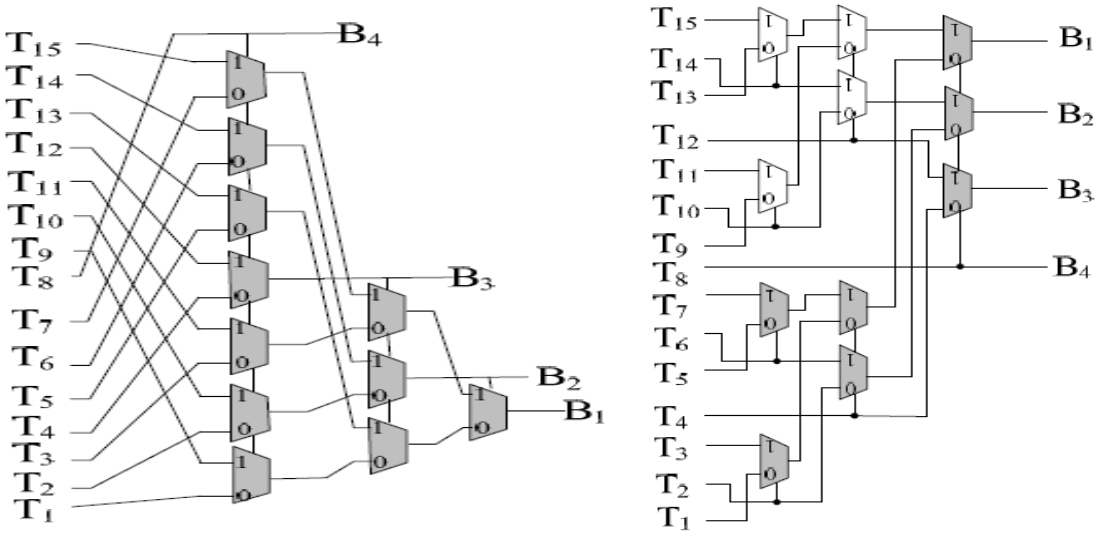

Fig.8: MUX based encoders

IV. PROPOSED HETEROGENEOUS ENCODER

Heterogeneous encoder can be implement from the any of existing encoders like Wallace tree encoder or Fat tree encoder. Heterogeneous encoder consists of full adder and multiplexer circuit as shown in fig 10. In this selection signal is used form MUX, which is critical. This can tolerant the bubble error and remaining signal can be used as inputs. Wallace encoder is also free from bubble error but it is complex in circuit. Hence, the proposed heterogeneous encoder is easy to design and also it consumes less power.

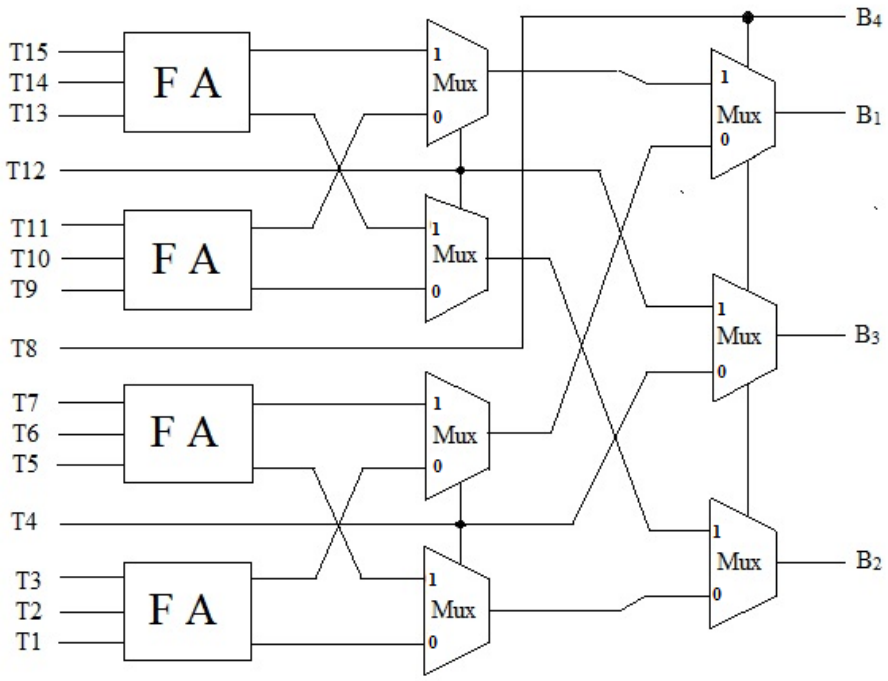

Fig.10: Proposed 4-bit Heterogeneous encoder

V. SIMULATION RESULTS

Simulation of heterogeneous encoder is performed using 0.18 µm CMOS technology in Cadence tool. The comparator consumes less power due to its small size and less number of transistor.

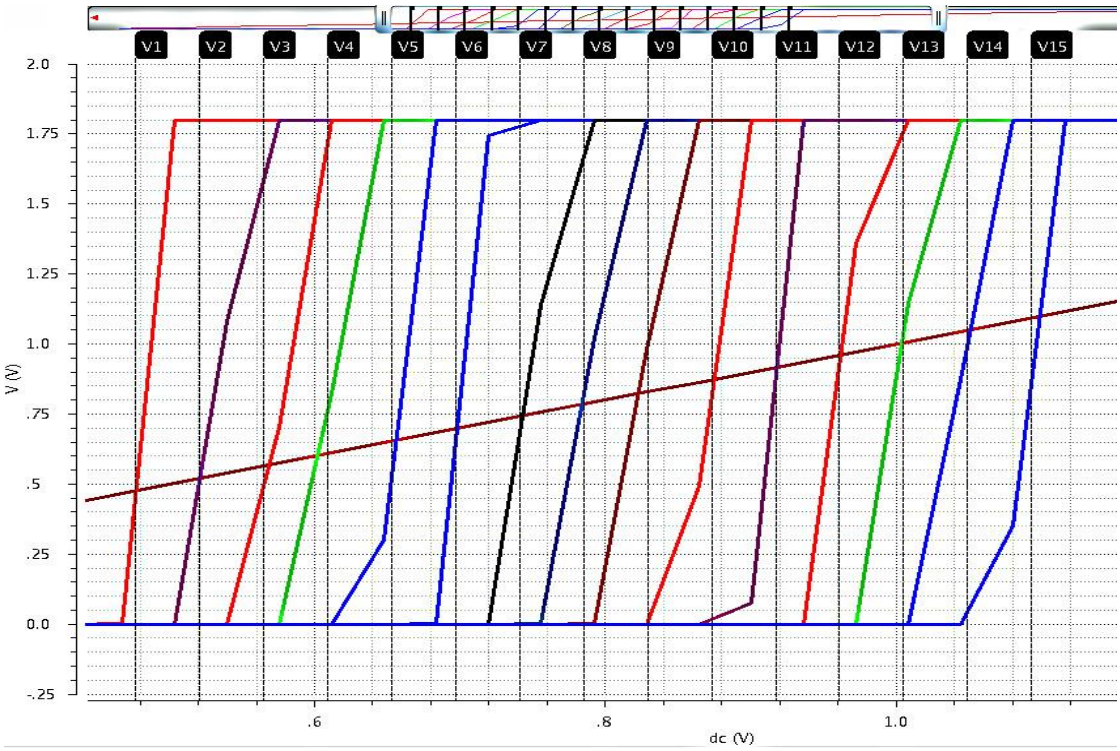

Fig.11: VTC of TIQ comparator block

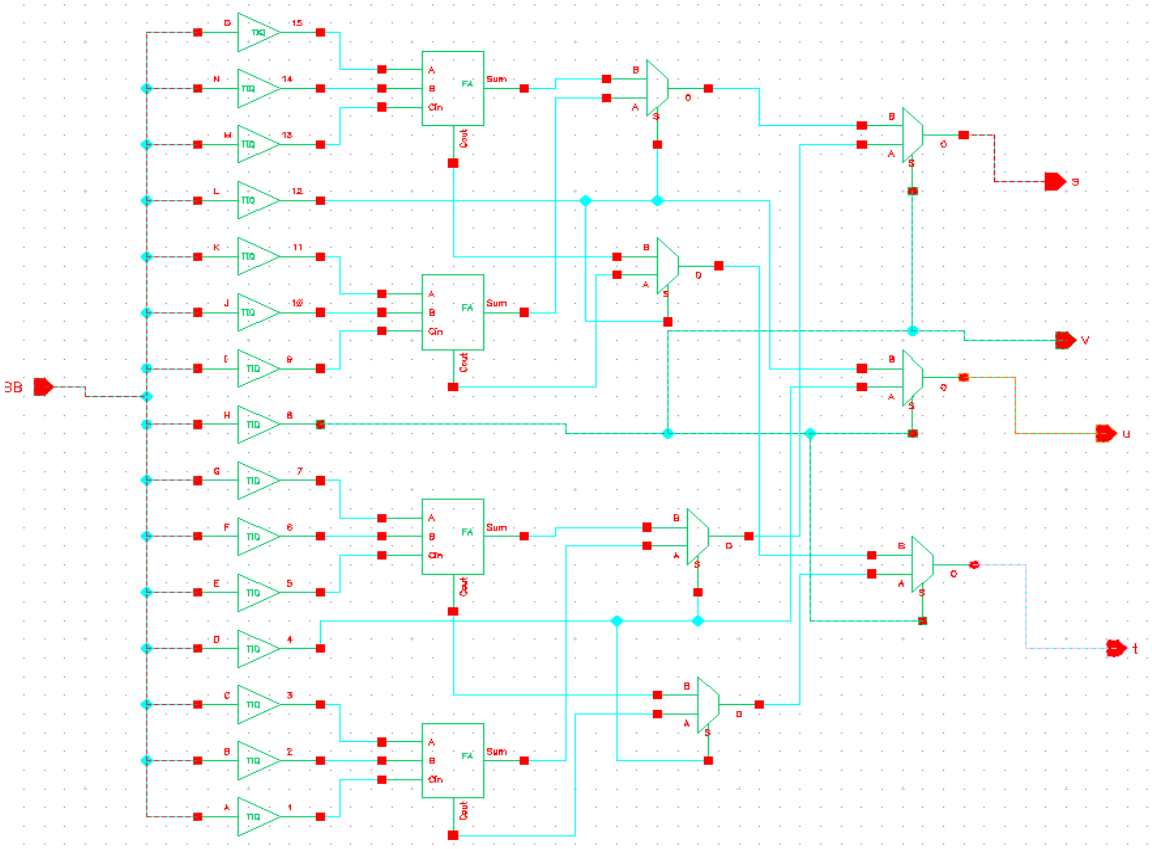

Fig.12: Schematic diagram of 4-bit Heterogeneous encoder

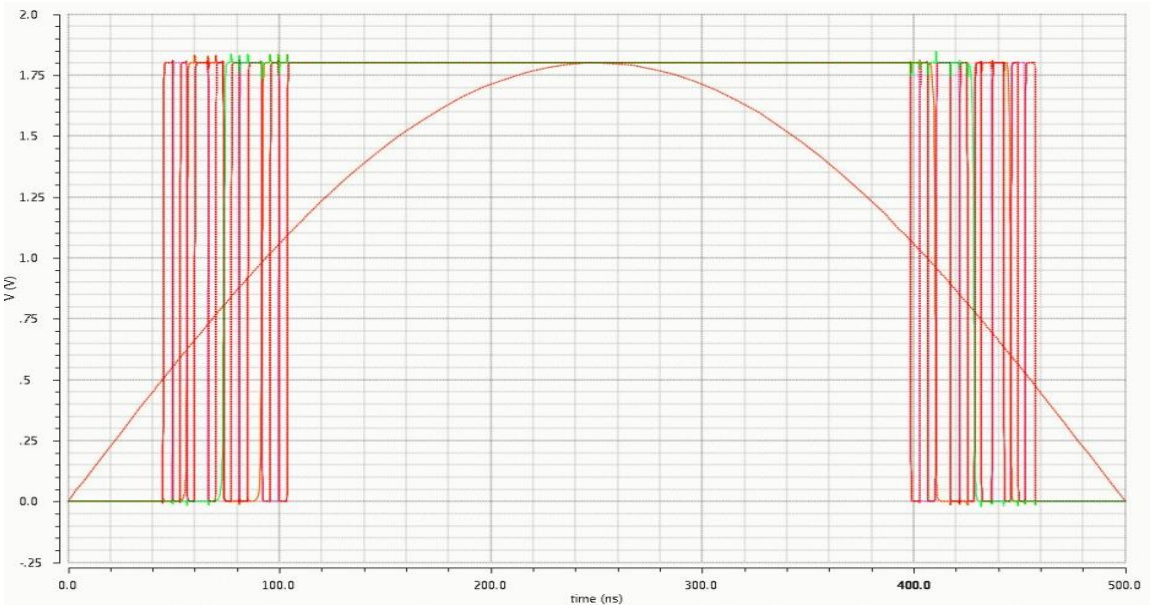

Fig.13: Transient response of comparator

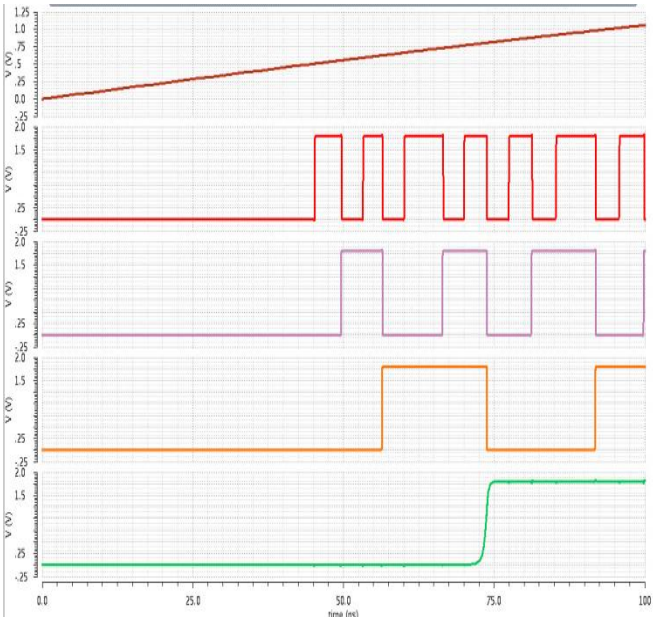

Fig.14: Digital output of 4 bit TIQ ADC using encoder of ramp input.

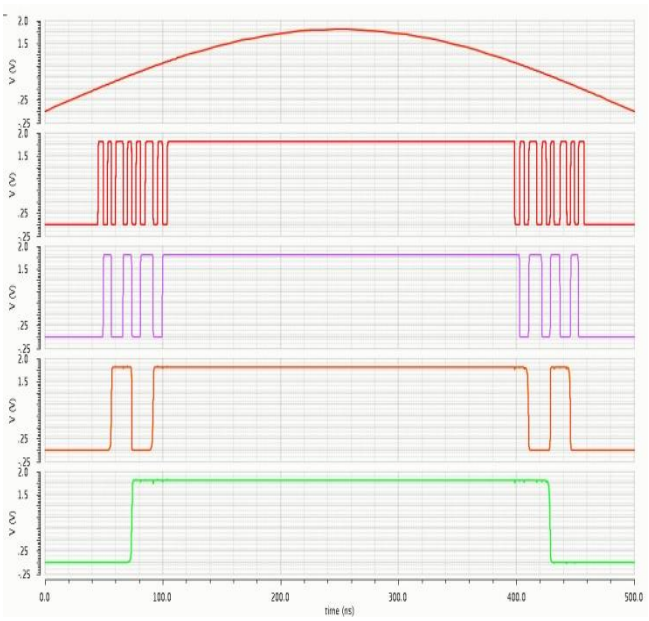

Fig.15: Digital output of 4 bit TIQ ADC using heterogeneous Heterogeneous encoder of analog input

VI. CONCLUSION

Now a day the growth of portable device and battery operated device like cell phone, laptops, tablet etc has increased. Hence the device should be design like that consume less power and have minimal area and the device can be operated for the long time. TIQ removes the array of resistors that makes the ADC devices to operate faster and it takes less area. As the discussed above Wallace tree takes more power, area and also has large delay compared to other architectures. Where Fat-Tree based encoder has less delay then the Wallace tree based encoders but falls between the MUX based encoder and Improved MUX based encoder. The area of the MUX based encoder and improved MUX based encoder are the same but improved MUX based encoder has less delay because it remove the huge fan-out from its critical path. MUX based encoder has more delay due to huge fan-out in its critical path. Both architecture have equal number of gates due to this power dissipation are the same for MUX based encoder and improved MUX based encoder. In this paper a new 4-bit heterogeneous encoder is proposed. This design removes the complexity of circuit and also it is beneficial in suppressing the bubble error. The experiment implementation is performed using 0.18µm CMOS technology in Cadence tool.

TABLE I: SIMULATION RESULTS OF 4-BIT TIQ ADC USING HETEROGENEOUS ENCODER

Features	Specification
Resolution	4-bit
Power supply	1.8v
Technology	180nm
Total power consumption	167.9E-6w
Propagation Delay	3.104E-9s

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